IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Currently Amended) A processor comprising:

a prediction circuit configured to predict an execution latency of a floating point operation responsive to a predicted precision of the floating point operation;

a register file;

a scheduler coupled to the register file and configured to schedule the floating point operation for execution, wherein the scheduler is configured to transmit one or more register addresses of operands of the floating point operation to the register file responsive to scheduling the floating point operation for execution, and wherein the prediction circuit is configured to predict the execution latency prior to the floating point operation being scheduled by the scheduler for execution; and

a floating point unit coupled to receive the floating point operation scheduled by the scheduler for execution and one or more operands read from the register file in response to the one or more register addresses received by the register file from the scheduler, wherein the floating point unit is configured to detect a misprediction of the execution latency.

2. (Currently Amended) The processor as recited in claim 1 wherein the predicted precision is a prediction of a precision of the operands of the floating point operation.

3. (Previously Presented) The processor as recited in claim 2 wherein the floating point unit comprises a control register storing a precision control indication indicative of an output precision for the floating point operation, wherein the predicted precision is the

output precision.

4. (Original) The processor as recited in claim 2 wherein the floating point operation is a multiply operation, and wherein the floating point unit comprises a multiplier designed for a first precision less than a maximum precision supported by the processor, and wherein the execution latency is based on a number of passes through the multiplier used to complete a multiplication of the precision of the operands.

5. (Original) The processor as recited in claim 2 wherein the floating point unit comprises a precision check circuit coupled to receive the operands of the floating point operation, wherein the precision check circuit is configured to detect the misprediction if at least one of the operands of the floating point operation has a precision that exceeds the predicted precision.

6. (Previously Presented) The processor as recited in claim 1 wherein the floating point unit is configured to signal the scheduler responsive to detecting the misprediction.

7. (Original) The processor as recited in claim 6 wherein the scheduler is configured to reschedule the floating point operation responsive to the signaling from the floating point unit with the execution latency indicated as a latency detected by the floating point unit.

8. (Original) The processor as recited in claim 6 wherein the prediction circuit is configured to predict the execution latency of the floating point operation responsive to dispatch of the floating point operation to the scheduler.

9. (Original) The processor as recited in claim 6 further comprising a trace cache configured to store predicted operation traces, wherein the prediction circuit is configured to predict the execution latency responsive to the floating point operation being included in a trace, and wherein the trace cache is configured to store an indication of the execution latency predicted by the prediction circuit.

10. (Original) The processor as recited in claim 9 wherein the trace cache is configured to store a selected opcode of at least two opcodes for the floating point operation responsive to the execution latency predicted by the prediction circuit, the selected opcode comprising the indication of the execution latency.

11. (Original) The processor as recited in claim 1 wherein the floating point unit is configured to signal an exception responsive to detecting the misprediction.

12. (Original) The processor as recited in claim 11 wherein the processor is configured to refetch the floating point operation responsive to the exception.

13. (Original) The processor as recited in claim 1 wherein the floating point unit is configured to detect the misprediction responsive to detecting an actual execution latency greater than the execution latency predicted by the prediction circuit.

14. (Original) The processor as recited in claim 13 wherein the floating point unit is configured not to detect the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted by the prediction circuit.

15. (Original) The processor as recited in claim 13 wherein the floating point unit is further configured to detect the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted by the prediction circuit.

16. (Currently Amended) A method comprising:

predicting an execution latency of a floating point operation responsive to a predicted precision of the floating point operation;

scheduling the floating point operation from a scheduler for execution in a floating point unit, wherein scheduling the floating point operation comprises transmitting one or more register addresses of operands of the

floating point operation to a register file to read one or more operands of the floating point operation, and wherein the predicting is performed prior to the scheduling; and

the floating point unit detecting a misprediction of the execution latency.

17. (Currently Amended) The method as recited in claim 16 wherein the predicted precision is a prediction of a precision of the operands of the floating point operation.

18. (Original) The method as recited in claim 17 wherein the floating point operation is a multiply operation, and wherein the floating point unit comprises a multiplier designed for a first precision less than a maximum precision supported by the processor, and wherein the execution latency is based on a number of passes through the multiplier used to complete a multiplication of the precision of the operands.

19. (Original) The method as recited in claim 17 wherein detecting the misprediction comprises detecting that at least one of the operands of the floating point operation has a precision that exceeds the predicted precision.

20. (Original) The method as recited in claim 16 further comprising rescheduling the floating point operation responsive to detecting the misprediction, with the execution latency indicated as a latency detected by the floating point unit.

21. (Original) The method as recited in claim 16 further comprising:

signaling an exception responsive to detecting the misprediction; and

refetching the floating point operation responsive to the exception.

22. (Original) The method as recited in claim 16 wherein detecting the misprediction comprises detecting an actual execution latency greater than the execution latency

predicted in the predicting.

23. (Original) The method as recited in claim 22 further comprising not detecting the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted in the predicting.

24. (Original) The method as recited in claim 22 further comprising detecting the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted in the predicting.